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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Title: **NON-VOLATILE MEMORY CELL COMPRISING DIELECTRICLAYERS HAVINF A LOW DIELECTRIC CONSTANT AND CORRESPONDING MANUFACTURING PROCESS**

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CERTIFICATE OF MAILING

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RESPONSE TO RESTRICTION REQUIREMENT

August 1, 2005

TO THE COMMISSIONER FOR PATENTS:

This communication is in response to the Restriction Requirement dated July 1, 2005 in which the Examiner restricted the pending claims in the present patent application.

The Examiner has restricted the claims into six groups: Group 1 claims 1-6 and 15-26 (Group 1), claim 5 (Group 1A), claim 6 (Group 1B), claims 7-14 and 27-30 (Group

2), claim 12 (Group 2A), claim 13 (Group 2B). As discussed below, the Applicants respectfully traverse the restriction requirement on the grounds that the Examiner can search and examine the entire application without serious burden. Although the Applicants traverse the restriction requirement as discussed below, they provisionally elect to prosecute Group I claims 1 – 6 and 15 - 26 if the Examiner does not withdraw the restriction requirement.

According to MPEP § 803, if the Examiner can search and examine the application without serious burden, then he/she **MUST** examine the application on the merits even though it includes claims to independent or distinct inventions. As discussed below, because claims 1 – 30 recite similar subject matter, the Examiner can perform a single search and examination that will cover all of the claims. Consequently, the Examiner can search and examine the application without serious burden, and, therefore, **MUST** examine all of the claims 1 – 30 together.

More specifically, claim 1 recites:

1. A non-volatile memory cell integrated on a semiconductor substrate and comprising:

a floating gate transistor including a source region and a drain region, a gate region projecting from the substrate and comprised between said source and drain regions, said gate region having a predetermined length and width and comprising a first floating gate region and a control gate region,

characterised in that said floating gate region is insulated laterally, along the width direction, by a dielectric layer with low dielectric constant value.

Claim 7 recites:

7. A process for manufacturing non-volatile memory cells on a semiconductor substrate organized in rows and columns to form a memory cell matrix, comprising the following steps:

form active areas in said semiconductor substrate bounded by an insulating layer,

form on said active areas a first dielectric material layer,

deposit a first conductor material layer on said first dielectric material layer,

define through a standard photolithographic technique a plurality of floating gate regions in said first conductor material layer,

characterised in that it comprises the following steps:

form a dielectric layer with low dielectric constant value on said floating gate regions.

Claim 16 recites:

16. A memory-cell structure formed on a semiconductor substrate, the memory-cell structure comprising a plurality of non-volatile memory cells arranged in rows and columns and formed on the semiconductor substrate, each memory cell including a floating gate region and the memory-cell structure including an insulating region having a relatively low dielectric constant formed between adjacent floating gate regions of memory cells in respective rows of the structure.

Claim 24 recites:

24. An electronic system, comprising:

a memory device including,

a memory-cell array formed on a semiconductor substrate, the memory-cell array comprising a plurality of non-volatile memory cells arranged in rows and columns and formed on the semiconductor substrate, each memory cell including a floating gate region and the memory-cell array including an insulating region having a relatively low dielectric constant formed between adjacent floating gate regions of memory cells in respective rows of the array.

Claim 27 recites:

27. A method of forming an array of memory cells on a semiconductor substrate, the method comprising:

forming a plurality of memory cells on the substrate and arranged in rows

and columns, each memory cell including a respective floating gate region; and

forming a first dielectric region between the floating gate regions of adjacent memory cells in respective rows of memory cells, the first dielectric layer having a relatively small dielectric constant.

The Examiner can perform a single search for claims 1 – 30. Furthermore, because these claims recite related subject matter, examination of these claims will involve similar analyses. Therefore, it is only slightly more burdensome for the Examiner to search and examine claims 1 – 30 than it would be for him/her to search and examine the provisionally elected Group I claims 1 – 6 and 15-26. Consequently, because there is no serious burden on the Examiner to search and examine all of the claims 1 – 30, the **restriction is improper**. Therefore, the Examiner **MUST** withdraw the restriction and examine all of the claims. Therefore, the Applicants respectfully request the Examiner to withdraw the restriction requirement and to examine all of the claims 1 - 30.

If the Examiner believes that a phone interview would be helpful, he is respectfully requested to contact the Applicants' attorney, Paul F. Rusyn, at (425) 455-5575. In the event an additional fee is due for this Response, you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

Respectfully submitted,

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